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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,700	RHODES ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-14,16,18,19 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-14, 16, 18, 19, and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-14, 16, 18, 19, and 22 are pending in the instant application.

Response to Amendment

2. In view of Applicant's amendments to the claims submitted March 13, 2006, new prior art rejections are set forth below.

Claim Objections

3. Claims 1-9, 11-14, 16, 18, 19, and 22 are objected to because of the following informalities:

Regarding claim 1, the claim is objected to because one is unable to determine the meaning of "connected in parallel at the first end" in lines 11-12 because parallel connections are made at two ends. Further, one is unable to determine if the diodes and inductors are connected at both ends or not because the inductors are seemingly coupled to the diodes at one end and to a control node at the other.

Regarding claim 14, the claim is objected to because one is unable to determine the meaning of "being bypassed" in line 11, and it makes the claim indefinite.

Regarding claim 19, the claim is objected to because it is dependent upon claim 15 which is cancelled.

Regarding claim 22, the claim objected to because one is unable to determine the meaning of "connected in parallel at the first end" in lines 3-4 because parallel connections are made at two ends. Further, one is unable to determine if the diodes and inductors are connected at both ends or not because the inductors are seemingly coupled to the diodes at one end and to a control node at the other.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 14, 16, 18, 19, and 22 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 14, the claim is indefinite because one skilled in the art is unable to determine the meaning of "the respective capacitor" in line 18. One is unable to determine any association for "the respective capacitor" which is definite. Furthermore, one is unable to determine which inductors are in the "subset of the first set of inductors" in line 17 because one is unable to determine which indictors are coupled to ground only by "the respective capacitor". That is, one is unable to determine if an inductor is coupled to one capacitor or more than one capacitor. Likewise, some of the plurality of capacitors that each inductor may be coupled to may or may not be connected to a notch filter. Therefore, one is unable to definitely determine which inductors are coupled to which capacitors that determines the appropriate category (the set or subset) of inductors. It should be additionally noted that use of the term coupled requires that every component is, at least indirectly, coupled to every other component.

Regarding claims 16, 18, 19, and 22, the claims are rejected for being based upon a rejected parent claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C.§ 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 7, 8, 11, 14, 16, 18, and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Atokawa (US 6414566 – previously cited) in view of Shimo (US 5193218 – previously cited) and in further view of Osofsky et al (US 6724840; hereafter "Osofsky" – previously cited).

Regarding claim 1, Atokawa discloses a multi-mode bidirectional communications device, comprising: a diplexer (fig. 1, "DUPLEXER"; fig. 2) having a filter coupled between a first signal point (fig. 2, "ANT") and a second signal point (fig. 2, "RX"), a filter coupled between the first signal point and a third signal point (fig. 2, "TX"), a digital control input (fig. 2, ref. CONT1) connected in signal communication with he low-pass filter, and a notch filter (fig. 2, refs. D2 & LT2 and D1 &LT1) selectively coupled to the low-pass filter by the digitally control input in response to indicium of a desired spectral region (col. 2, lines 30-45; col. 5, lines 35-50), wherein said notch filter comprises only a plurality of inductors (fig. 2, refs. LT1 and LT2) and a plurality of PIN diodes (col. 5, lines 50-55; fig. 2, refs. D1 and D2), each of the plurality of inductors having a first end and a second end, each of the plurality of inductors connected in parallel with a respective one of the plurality of PIN diodes at the first end and a common control node at the second end. The common control node is the end of

inductors LT1 and LT2 which are coupled together. As broadly as claimed, the notch filter is comprised of only the specific plurality of inductors and capacitors noted (fig. 2, refs. D2 & LT2 and D1 &LT1). The purpose of the diplexer of Atokawa is to couple both a high frequency signal and a low frequency signal upon a single channel. Atokawa has a selectable "notch" filter (fig. 2, refs. D2 & LT2 and D1 &LT1) that may be variably coupled to the low pass filter by a control voltage (fig. 2, ref. "CONT1") in response to a desired spectral response of the filter (col. 4, lines 23-30). Atokawa does not explicitly disclose that the filter between the first and second signal points is a high pass filter and the filter between the first and third signal points is a low pass filter. However, Atokawa's filter between the first and second points is a high pass filter due solely to its component configuration as is understood by one having skill in the art. Furthermore, it is at least as much of a high pass filter as the one of the instant application (fig. 5) because both are comprised of the same configuration of components. Likewise, Atokawa's filter between the first and third signal points is a low pass filter for the same reasons.

Further regarding claim 1, Atokawa does not disclose that the communications device asserts the control voltage using a digitally operable switch responsive to signals from a microprocessor. However, Shimo teaches the use of digitally operable transistor switches (fig. 5, refs. 71 and 72) in signal communication with a control circuit (fig. 5, ref. 6) to modify a filter response (col. 2, lines 39-68). As understood by one having skill in the art, the transistor switches provide a digital interface to an analog circuit. That is, the switches allow for the analog filter to be controlled by a digital control circuit (fig. 5,

ref. 6; col. 4, lines 29-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a transistor switch and control circuit as taught by Shimo to assert the control pin of the communication device of Atokawa because it would allow for a low power digital control voltage from a control circuit to be interfaced with the analog portions of the communication device.

Further regarding claim 1, Atokawa in view of Shimo disclose a communication device with a digitally operable switch coupled to a control circuit, but do not explicitly disclose that the control circuit is a *microprocessor.* However, Osofsky teaches a microprocessor (fig. 1B, ref. 50) control circuit which digitally controls a tunable communications device (fig. 2) using digital control input pins (fig. 2, refs. D4, D3). As notoriously known by those having skill in the art, microcontrollers are advantageous controllers because they can be programmed to perform a multiplicity or various functions. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a microprocessor as taught by Osofsky as the control circuit in the communications device of Atokawa in view of Shimo because it is an effective and adaptable digital controller.

Regarding claim 2, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, Atokawa discloses upstream processing circuitry (fig. 1, "TRANSMITTER CIRCUIT") and downstream processing circuitry (fig. 1, "RECEIVER CIRCUIT") coupled to said diplexer.

Regarding claim 7, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, said high pass filter passes signals greater than 88Mhz (fig. 4).

Regarding claim 8, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, Atokawa discloses that said upstream processing circuitry (fig. 1, "TRANSMITTER CIRCUIT") is selectively coupled to one of said low-pass filter and said low-pass filter in conjunction with said notch filter (fig. 1, "TRANSMITTING FILTER"; fig. 2, filter between "ANT" and "TX").

Regarding claim 11, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 1 as applied above. Further, Shimo discloses that the digitally operable switch is a transistor as applied to claim 1 above.

Regarding claim 14, Atokawa discloses a high pass filter, a low pass filter, a digitally selectable switch, and a notch filter as applied to claim 1 above. Further Atokawa discloses by figure 2 that said low-pass filter comprises a first set of inductors (L1 and L2) connected in series between said first (ANT) and third signal ports (TX), each of said first set of inductors being coupled to ground via a respective capacitor (C3, C11, C21) from a set of capacitors forming thereby a plurality of single pole filter elements, a portion of said first set of inductors being bypassed by a subset of the set of capacitors (C20, C11), the portion consisting of any of the first set of inductors which are connected to said notch filter via any of the capacitors in the subset of capacitors, wherein said notch filter comprises a second set of inductors (LT1 and LT2), where each inductor is respectively coupled between a particular one of capacitors in the

subset of capacitors and ground, and wherein a subset of the first set of inductors (L1) are directly connected to ground via only the respective capacitor (C3) from the set of capacitors, the subset of the first set of inductors consisting of any inductors in the set of inductors that are directly coupled to any capacitors in the set of capacitors that are excluded from the subset of capacitors.

Regarding claim 16, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa discloses that said high-pass filter (fig. 2) comprises: a plurality of capacitors (fig. 2, refs. C34, C45) connected in series between said first (RX) and second signal ports (ANT), each of said capacitors being coupled to ground via serially coupled circuit elements (fig. 2, refs. L3 & C30, L5 & C50) forming thereby a plurality of single pole filter elements, each of said serially coupled circuit elements comprising a capacitor and inductor.

Regarding claim 18, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Shimo discloses that the selector switch is a transistor (fig. 5, ref. 71).

Regarding claim 22, Atokawa in view of Shimo, and in further view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa discloses the remaining limitations as applied to claim 1 above.

8. Claims 2, 3, 5, 6, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel et al (US 6804262; hereafter "Vogel" – previously cited) in view of Atokawa, in further view of Shimo, and in further view of Osofsky.

Regarding claim 2, Vogel discloses upstream processing circuitry (fig. 3, refs. 114, 120, and 106) and downstream processing circuitry (fig. 3, refs. 108, 112, 116, and 114) coupled to a diplexer (fig. 3, ref. 104). Vogel does not disclose that the diplexer is having a high-pass filter, a low-pass filter, and a notch filter selectively coupled to the low-pass filter in response to indicium of a desired spectral region. However, Atokawa teaches the limitations Vogel does not explicitly disclose as applied to claim 1 above. Atokawa teaches that, with the proposed variable bandwidth diplexer circuit, two passing bands are available for transmitting and receiving (col. 2, lines 22-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the diplexer circuit as taught by Atokawa in the communications device of Vogel because two pass bands of transmission and two pass bands of reception could be accommodated. Further, Shimo and Osofsky teach the digitally operable switch connected in signal communication with the low-pass filter and responsive to signals from a microprocessor as applied in the rejection of claim 1 as being unpatentable over Atokawa in view of Shimo, and in further view of Osofsky, above.

Regarding claim 3, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, Vogel discloses that the downstream processing circuitry comprises: a tuner (fig. 3, refs. 108); a demodulator (fig. 3, ref. 114; col. 10, lines 17-25); a first SAW filter (fig. 3, ref. 112; col. 9, lines 48-51) selectively coupled between said tuner and said demodulator; and a second SAW filter (fig. 3, ref. 116) selectively coupled between said tuner and

said demodulator (col. 9, lines 55-60). Vogel does not explicitly disclose that the second filter is of a SAW filter type, but it is implied that the second filter (116) is functionally equivalent to the first filter (112) because they are used for the same purpose and in the same manner.

Regarding claim 5, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, Vogel discloses at least one selector (fig. 3, ref. 110) for selectively coupling the first SAW filter and the second SAW filter between the tuner and the demodulator.

Regarding claim 6, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, in the communications device of Vogel in view of Atokawa, the tuner begins the downstream channel of the receiver

Regarding claim 12, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 as applied above. Further, the device of Vogel in view of Atokawa is a cable modem as disclosed by Vogel (col. 2, lines 12-20).

9. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky, and in further view of Miner et al (US 6690655; hereafter "Miner" – previously cited).

Regarding claim 4, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 3 as applied above. Further, Vogel discloses that the bandwidth of the first SAW filter is 6Mhz (col. 9, lines 49-50).

Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky do not explicitly disclose that the second filter has a bandwidth of 8Mhz but discloses that the second filter changes the bandwidth of the first filter such that a second frequency selection system is defined (col. 9, lines 55-68). Vogel also discloses that various modifications of the frequency selection system may be made and suggests that the second filter and the first filter may be connected in parallel rather than in series (col. 10, lines 1-9). Additionally, Miner teaches that the fundamental difference in the Data-Over-Cable System Interface Specification (DOCSIS) system which is specified by Vogel (col. 2, lines 12-20) between domestic and international versions is the downstream channel bandwidth which is 6Mhz in the United States and 8Mhz internationally (col. 6, lines 10-11). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the domestic and international bandwidth spectra (6Mhz and 8 Mhz, respectively) as taught by Miner for the frequency selection system of Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky because the multi-mode bi-directional communications device could thereby the used both in the United States and abroad.

Regarding claim 13, Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky, and in further view of Miner disclose the limitations of claim 4 as applied above. Further, the device of Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky disclose, and in further view of Miner supports the domestic (North American) DOCSIS as well as international (European) DOCSIS as applied to claim 4 above.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vogel in view of Atokawa, in further view of Shimo, in further view of Osofsky, and in further view of Wilson et al (US 2002/0159511; hereafter "Wilson" – previously cited).

Regarding claim 9, Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky disclose the limitations of claim 2 (taking all the limitations of claim 1) as applied above. In the device of Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky, the frequency bands of the low pass filter and the low pass filter coupled to the notch filter are not explicitly disclosed. However, Vogel does disclose that the low pass filter should have an operable range of 5 to 42 Mhz depending on the operation of the device (col. 7, lines 20-25) but is not limited to such an operating range. One skilled in the art would find it obvious that the operating range of a variable frequency low pass filter should accommodate all possible frequency ranges which may be desirable. In the DOCSIS device of Vogel in view of Atokawa, at least two frequency ranges for the low pass filter are available. Vogel in view of Atokawa, in further view of Shimo, and in further view of Osofsky does not disclose expressly passing signals less that 65Mhz as a possible selectable pass-band frequency range. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to utilize any other frequency range applicable to the device (i.e. 65Mhz). Applicant has not disclosed that the use of a 65Mhz low pass filter pass-band range provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a 65Mhz low pass filter

pass-band range as taught by Wilson (para. 0046) because it is readily utilized in a data over cable system as taught by Wilson (para. 0012). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a 65Mhz low pass filter pass-band as taught by Wilson in the device of Vogel in view of Atokawa-'566 because it is readily applicable to data over cable systems.

11. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atokawa in view of Osofsky.

Regarding claim 14, Atokawa discloses a high pass filter, a low pass filter, and a notch filter as applied to claim 1 above. Atokawa also discloses a digitally operable switch (fig. 2, refs. D1 and D2) connected in signal communication with said low-pass filter. Osofsky discloses that the switch of Atokawa may be advantageously controlled by signals from a microprocessor as applied to claim 1 above. Further Atokawa discloses by figure 2 that said low-pass filter comprises a first set of inductors (L1 and L2) connected in series between said first (ANT) and third signal ports (TX), each of said first set of inductors being coupled to ground via a respective capacitor (C3, C11, C21) from a set of capacitors forming thereby a plurality of single pole filter elements, a portion of said first set of inductors being bypassed by a subset of the set of capacitors (C20, C11), the portion consisting of any of the first set of inductors which are connected to said notch filter via any of the capacitors in the subset of capacitors, wherein said notch filter comprises a second set of inductors (LT1 and LT2), where each inductor is respectively coupled between a particular one of capacitors in the subset of capacitors and ground, and wherein a subset of the first set of inductors (L1)

are directly connected to ground via only the respective capacitor (C3) from the set of capacitors, the subset of the first set of inductors consisting of any inductors in the set of inductors that are directly coupled to any capacitors in the set of capacitors that are excluded from the subset of capacitors.

Regarding claim 19, Atokawa in view of Osofsky disclose the limitations of claim 14 as applied above. Further, Atokawa discloses that the digitally operable switch comprises a plurality of PIN diodes (fig. 2, refs. D2 and D1; col. 5, lines 50-55) respectively coupled in parallel with said second plurality of inductors (fig. 2, refs. LT1, LT2), wherein said PIN diodes are adapted for connection to a control signal (CONT1) from the microprocessor (Osofsky; fig. 1B, ref. 50) for selectively biasing the PIN diodes to couple and decouple the notch filter to the low-pass filter.

Allowable Subject Matter

12. No claims are allowed.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Jason M. Perilla
May 8, 2006

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER